AMENDMENTS

Please amend the above-referenced application as follows:

IN THE TITLE:

Please substitute the following clean-text title for the pending title.

AN APPARATUS AND METHOD FOR PERFORMING SINGLE-INSTRUCTION MULTIPLE-DATA INSTRUCTIONS

IN THE SPECIFICATION:

Please substitute the clean-copy specification as found in Appendix B for the pending specification. Appendix C contains an annotated version of the specification and the abstract.

IN THE CLAIMS:

Please substitute the following clean-copy text for the pending claim of the same number. Appendix A contains an annotated version of the claims.

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1. (Amended) An apparatus for performing single-instruction multiple-data instructions using a single multiply-accumulate (MAC) unit, comprising:

a MAC unit configured to generate a data result, the data result having a first half and a second half;

a register communicatively coupled to the multiply-accumulate unit, the register configured to store the first half of the data result; and

a miscellaneous-logic unit configured to initiate the release of the first half of the data result from the register to synchronize the first half of the data result with the second half of the data result.

2. (Amended) The apparatus of claim 1, wherein said MAC unit generates the first half of the data result before the second half of the data result.

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3. (Amended) The apparatus of claim 2, further comprising:

a register file configured to receive the first half of the data result substantially concurrently with the second half of the data result.

4. (Amended) The apparatus of claim 3, wherein said miscellaneous-logic unit generates an exception result when said miscellaneous-logic unit determines the first half of the data result is erroneous.

5. (Amended) The apparatus of claim 4, wherein said miscellaneous-logic unit is configured to initiate the release of one of the first half of the data result stored in said register or initiate the release of the exception result.

6. (Amended) A method for performing single-instruction multiple-data instructions using a single multiply-accumulate unit , comprising:

providing a multiply-accumulate unit configured to generate a first half of a data result and a second half of a data result;

applying the first half of the data result at an input of a register;

using a miscellaneous-logic unit to generate an exception result; and

applying the first half of the data result and the second half of the data result at an input of a buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are valid, otherwise applying an exception result at the input of the buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are invalid.

7. (Amended) The method of claim 6, further comprising:

latching a first operand into said MAC unit; and

latching a second operand into said MAC unit.

8. (Amended) The method of claim 7, further comprising:

generating the first half of the data result from the first operand; and

generating the second half of the data result from the second operand.

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9. (Amended) The method of claim 8, further comprising:

latching the first half of the data result in a miscellaneous logic unit; and

latching the second half of the data result in the miscellaneous logic unit.

10. (Amended) The method of claim 9, further comprising:

generating the exception result from the first half of the data result and the second half of the data result.

11. (Amended) An apparatus for performing single-instruction multiple-data instructions, comprising:

means for generating a first data result responsive to a first operand;

means for storing the ~~first data~~ result;

means for generating a second data result responsive to a second operand;

means for generating an exception result responsive to the first and second data results;

means for forwarding the first data result and the second data result to a buffer when the exception result indicates that the first data result and the second data result are valid; and

means for communicating the exception to the buffer when the means for forwarding indicates that the first and second data results are invalid.

12. (Amended) The apparatus of claim 11, further comprising:

means for storing the first operand; and

means for storing the second operand.

Please cancel claims 13, 14, and 15 without prejudice , waiver, or disclaimer.